WHAT IS CLAIMED IS:

1. An information processing device comprising:

an m×n (m-row x n-column) instruction buffer;

a plurality of instruction executing parts executing a plurality of instructions in parallel; and

a control circuit selecting a predetermined number of instructions from said m×n instruction buffer and distributing said instructions to said instruction executing parts.

2. The information processing device as claimed in claim 1, wherein said control circuit comprises n selection circuits, each of said selection circuits selecting an instruction from m instructions of the corresponding column.

3. The information processing device as claimed in claim 1, wherein said control circuit comprises n selection circuits and a control part controlling said selection circuits, said control part controlling said selection circuits by referring to information included in each instruction indicating whether the instruction is simultaneously executable so as to select an

instruction from m instructions of the corresponding column.

4. The information processing device as claimed in claim 1, wherein said control circuit comprises;

n first selection circuits;

a 1×n (1-row x n-column) buffer holding a predetermined number of instructions selected by said first selection circuits; and

a second selection circuit distributing said instructions held in said 1×n buffer to said instruction executing part.

5. The information processing device as claimed in claim 4, wherein said first selection circuits selects instructions based on first information included in each instruction, said first information indicating whether the instruction is simultaneously executable, and said second control circuit selects instructions based on second information included in each instruction, said second information indicating a type of instruction of the instruction.

6. The information processing device as claimed in claim 1, wherein said control circuit selects only the instructions which satisfy at least

one predetermined condition.

7. The information processing device as claimed in claim 6, wherein said predetermined instructions include conditions related to a length of instruction or a combination of instructions.

8. The information processing device as claimed in claim 1, wherein said instruction executing part includes a plurality of slots and said control circuit includes n first selection circuits and a 1×n (1-row x n-column) buffer holding a predetermined number of instructions selected by said first selection circuits, and

wherein the number of said plurality of slots being greater than or equal to the number of said 1×n (1-row x n-column) buffers holding n instructions.

9. The information processing device as claimed in claim 1, wherein said m×n instruction buffer receives a group of instructions read out from a memory which does not include any NOP instruction.

10. A computing system comprising a memory storing instructions and a processor parallel processing said instructions read out from said memory,

wherein said processor includes;

an m×n (m-row x n-column) instruction buffer;

a plurality of instruction executing parts executing a plurality of instructions in parallel; and

a control circuit selecting a predetermined number of instructions from said m×n instruction buffer and distributing said instructions to said instruction executing parts.